

The Finite Element Analysis of Influence of Heat Transfer in Material Components of Solder Bumps

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Abstract

Deformation of components in IC die packages with the heat transfer in material components of solder bumps is investigated by finite element analysis (ANSYS). The composite of materials is studied separately by the simulation that is similar to the condition applied in the HDD industry. It is shown that tin is responded to temperature slower than other composite materials. When material composite is inconsistently mixed in the solder bump, there is high possibility of fatigue life in solder ball.

Keywords: finite element method, IC die package, solder bumps

Introduction

The better performance of hard disk drives (HDD) is important for the commercial competition. Many business companies attempt to develop HDD in order to be the leader in this industry. Every part in HDD has been developed for the better performance, for example smaller volume, higher capacity and faster data reading - writing. IC packages have also been developed to have thinner package size, smaller volume, and better thermal and electrical performance.

Many research literatures have been dedicated to study flip-chip performance factors. Charles (1990) and Shah (1990) reported the influence of geometry solder profile on the fatigue life during the temperature cycle. Heinrich and

colleague (1993) have developed the predicted models for area-array type solder joints on basic of analytical algorithm. Suhir (1993) studied thermal matching assembly particularly in the mechanical behavior and stated that appreciable reduction in the stress-strain level can be the result of an increase in the solder bump height-to-diameter ratio. Lau and Pao (1996) found that solder bumps with underfill were more reliable than solder bumps without underfill because the stress of solder bumps without underfill increased sharply from inside to outside.

Since finite element analysis has been dominated in material property areas, the finite element method has been applied in the HDD development in order to improve HDD performance. Pang and colleague (Pang and colleague,1997) used 2D and

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3D finite element models of the flip-chip assembly to study the effect of curing-induced bending stress in the silicon chip. They reported that there was no difference between 2D and 3D finite element simulation. However, 2D finite element simulation provided shorter time calculation. Teo (1998) investigated the influence of solder bump material, chip size, pad options and underfill material under effected conditions, such as temperature cycle, power circulation, stable temperature, humidity test and high temperature test. Significantly, the research has shown that the fatigue damage in solder bump was caused mostly by the loading temperature. Furthermore, Liu (2000) proposed the novel technique which is named hybrid method. Their technique is a combination between analytical algorithm and energy-based method to forecast the force balanced surface profile and restoring forces of solder joints in multiple pad shape area package. Wu (2005) studied the thermo mechanical behavior in flip-chip packages by 3D finite element analysis. The maximum equivalent stress and strain on the solders were considerably found at the corner solders. Jong(2005) investigated the geometrical effects of bumps on the fatigue life of flip-chip package by Taguchi method and found that the influence of climbing height of underfill was significant to the fatigue life assessment of flip-chip bumps and the width of the solder bump was the most important factor.

Theory and Analysis

Heat transfer of material property is significant to the heat reflow in solder bump of IC die package.

$$\dot{Q}_x = -KA \frac{dT}{dx} \tag{1}$$

$$Q_x'' = -K \frac{dT}{dx} \tag{2}$$

Where K Thermal Conductivity ($W/m \cdot k$), Heat Transfer Ratio, Q_x' Heat Flux Ratio (per area unit), $\frac{dT}{dx}$ Temperature Difference, A Area of Plate and x Distance (m)

Finite Element Analysis

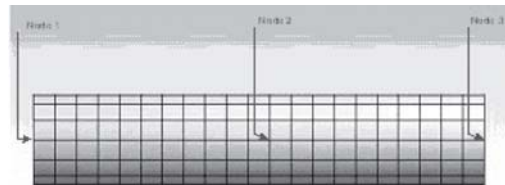


Figure 1. 2D finite element analysis of heat transfer solution

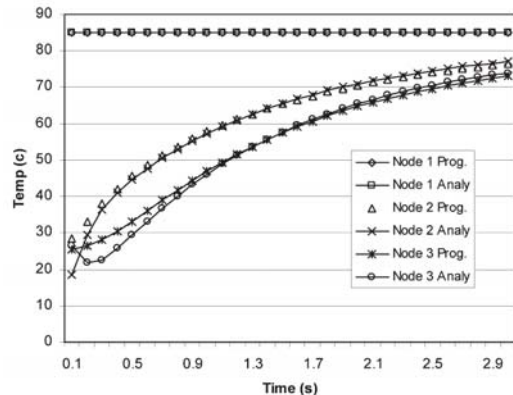


Figure 2. Resultant heat simulation

Figure 1 shows the example of mesh modeling and figure 2 shows the temperature in different nodes (elements) which is the heat characteristic in different levels when the heat source (85°C) start at node 1. Therefore, the node 2 and 3 are slowly heated and after 3 second every nodes are at the level of 85°C temperature. Figure 2 shows the general heat transfer characteristics.

A model of an IC die package was built to be used in this study. The major components of IC die package consist of preamp, solder bump and flex. In this study, the solder bump is focused. Figure 3 and 4 show the picture of an IC flip-chip package and dimensions of an IC die package, respectively.

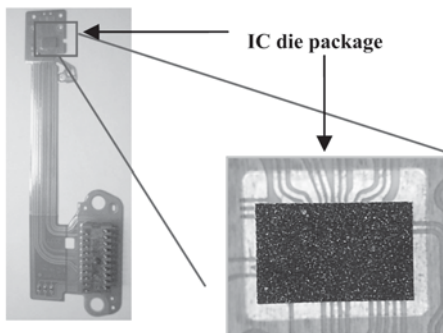


Figure 3. The example IC flip-chip package for this study

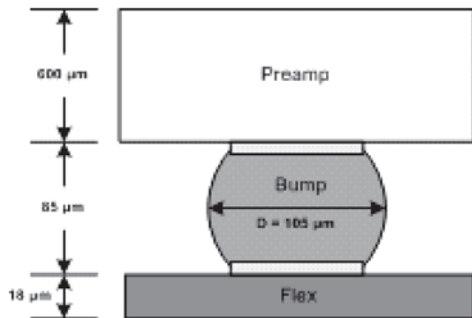


Figure 4. Dimensions and geometry of the IC die package

Table 1 shows three major components, i.e., tin (Sn), silver (Ag) and copper (Cu), which are studied. Table 1 shows material properties for simulating in the finite element analysis.

Table 1. Material Properties

Property	Material			
	Copper (Cu)	Silicon (Si)	SAC	Air
Young modulus (Pa)	1.30E+11	1.07E+11	25-46	-
			50-44	
			100-35	
Poisson's ratio	0.33	-	0.4	-
Density (kg/m ³)	8920	2330	7390	1.225
Thermal expansion (1/C)	1.65E-05	2.60E-06	2.35E+01	3.43E-03
Thermal conductivity (w/m c)	401	149	73.2	0.024
Specific heat (J/kg C)	385	700	226	100.35
Resistivity (ohm m)	1.68E-08		1.10E+01	
Melting point (C)	1084.62	1414	217	

* SAC = Sn95.5Ag3.8Cu0.7

The reflow machine was heated in order to melt bump and make it connect to substrate. Nitrogen was used to limit the amount of oxygen in the reflow machine, which was caused by the oxidation reaction. The machine was heated in 8 intervals.

Firstly, 2D modeling in ANSYS is built as its the actual size parameters following in figure 4. The actual parameters in solder bumps are also applied to the ANSYS. Figure 5 shows the 2D modelling with 308 elements and 2339 nodes and figure 6 shows the temperature potential distribution when the heat flows in one side. Therefore, the result shows the heat transfer characteristic that higher temperature always flow to lower temperature. Figure 7 shows the temperature potential distribution when the heat flows to both sides, top and bottom, which is the actual situation of heat reflow process in industry and the analysis is studied at different steps of 50, 100, 150 and 200°C. Figure 8 shows the comparison of different composites, which are Ag, Sn, SAC and Cu when each material is simulated as a solder bump in the ANSYS. There are significant results although the real composite of a solder bump is SAC405 which consists of Ag, Sn, SAC and Cu.

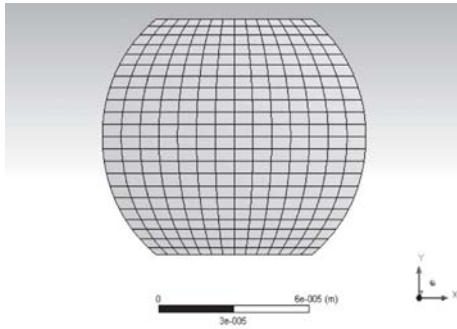


Figure 5. 2D Finite element mesh modeling

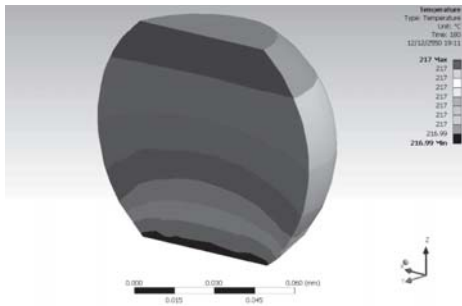


Figure 6. Inside temperature of a solder bump

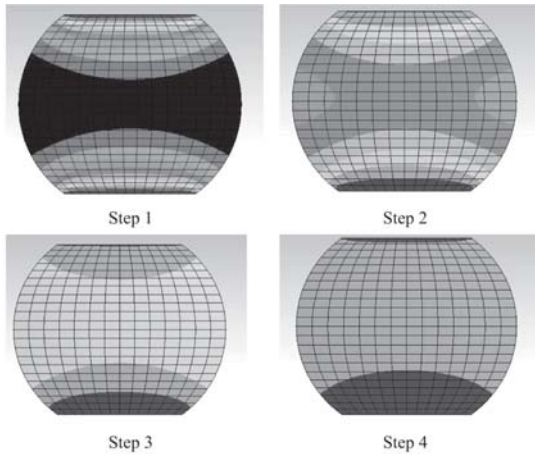


Figure 7. Finite element analysis on the solder bump

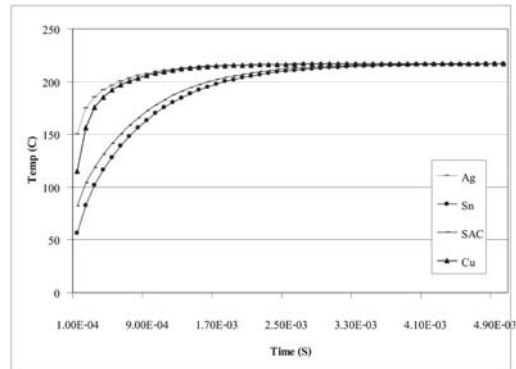


Figure 8. Comparison of composite in the solder bump

Conclusion

The results of this study show that material composite used in solder bumps has dramatically different heat transfer characteristics. It is shown that tin is responded to temperature slower than other composite materials. When material composite is mixed to a solder bump, there is high possibility of fatigue life in solder ball when the IC package is heated unevenly. However, the chip weight is also needed to be studied further because it is a main parameter of fatigue life of solder ball.

Acknowledgment

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References

- Liu, C. M. and Chiang, K. N. 2000. "Solder Shape Design and Thermal Stress/Strain Analysis of Flip Chip Packaging Using Hybrid Method." *Int'l Symp on Electronic Material & Packaging*, pp.44-50.
- Suhir, E. "Mechanical Behavior and Reliability of Flip Chip Solder Joint Interconnections in Thermally Matched Assemblies", in *Proc. 42nd Electron. Comp. Technol. Conf.*, 563-572.
- Wu, G. H., Tsein, T. C. and Ju, S. H. 2005. "Three-dimensional Finite Element Analysis of Thermomechanical Behavior in Flip-chip Packages under Temperature Cycling Conditions." *Journal of Reinforced Plastics and Composites*, p.1895-1907.
- Charles, H. K. and Clatterbaugh, G. V. 1990. "Solder Joint Reliability - Design Implications from Finite Element Modeling and Experimental Testing." *ASME Journal of Electronic Packaging Vol. 112, No.2* , pp. 135-146.
- Pang, H.L.J., Tan, T. I., Lim, G. Y. and Piscataway, N. J. "Thermal Stress Analysis of Direct Chip Attach Electronic Packaging Assembly", *IEEE Electronic Packaging Technology Conference*, pp.170-176.
- Lau, J. H. and Pao, Y. H. "Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies", McGraw-Hill, New York, NY.
- Teo, K. H. 1998. "Reliability Assessment of Flip Chip on Board Connections", *Proceeding of the IEEE/CPMT 2nd Electronic Packaging Technology Conference (EPTC'98)* , pp.269 - 273.
- Shah, M. K. 1990. "Analysis of Parameters Influencing Stress in the Solder Joint of Leadless Chip Capacitor." *ASME Journal of Electronic Packaging Vol. 118, No.3* , pp. 122-126.
- Wen-Ren Jong, Shia-Chung Chen, His-Chun Tsai, Chien-Chia Chiu and Hsiu-Tao Chang, 2005. "The Geometrical Effects of Bumps on the Fatigue Life of Flip-chip Packages by Taguchi Method", *Journal of Reinforced Plastics and Composite, Vol. 00, No. 00/2005*.
- Heinrich, S. M., Liedtke, P. E., Nigro, N. J., Elkouh, A. F. and Lee, P. S. 1993. "Effect of Chip and Pad Geometry on Solder Joint Formation in SMT." *Journal of Electronic Packaging Vol. 115*, pp. 433-439.

